Hitachi Programmable Controller

HIDIC H Series

COUNTER MODULE

Instruction Manual

TYPE : XCU001H | XCU232H

Notes
- Ensure that the person with the final responsibility for maintenance of the module has a copy of this instruction manual. The manual must be maintained in good order after use.
- Follow the items described in this document regarding the wiring and installation of this module. Advise personnel in charge of wiring regarding the information contained in the manual.

HITACHI

NJI-402X

About the separate account manual

As for the operation manual, manual with regard to this product, there is the following. As occasion demands, please ask this table of reference.

⚠ CAUTION

- Please read a detailed operation manual, manual, to use safely.
- Please confirm whether the operation manual, manual are a latest version.
- Please order the application manual, operation manual of separate account to agent, or our company sales.

Instruction manual, Operation manual

Name	Manual No.
COUNTER MODULE Instruction Manual (XCU001H)	NB973*X
2-CHANNEL COUNTER MODULE Instruction Manual (XCU232H)	NB3111*X

The alphabet of the end of manual No. (*: one letter) expresses the revision. The first edition is space.

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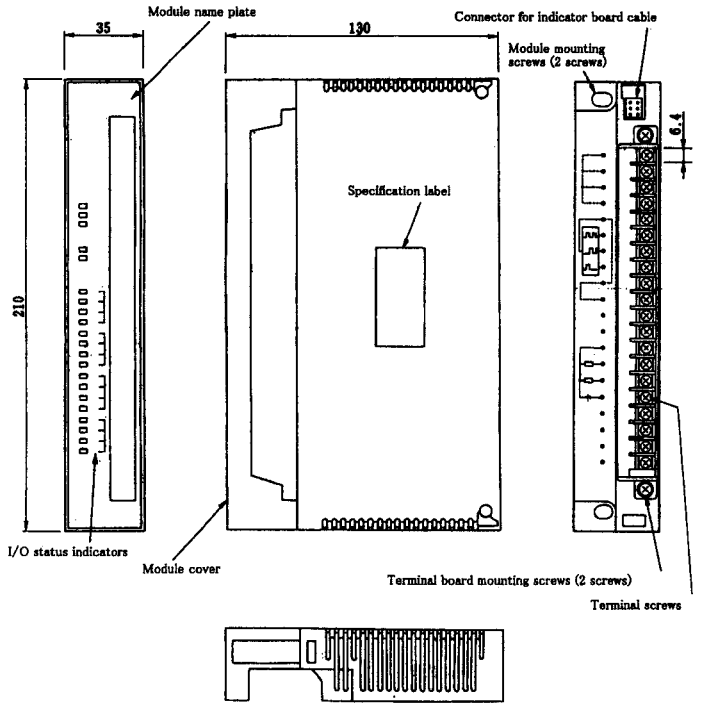
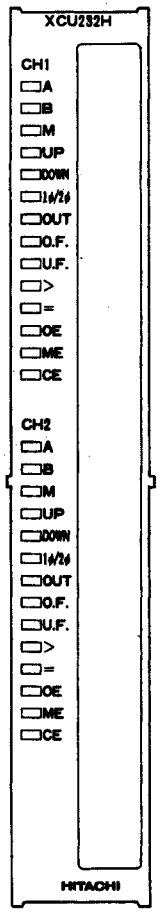
XCU001H

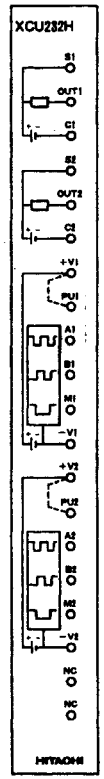


Note) This figure is expressing XCU001, although the same size even XCU232. Please see the next page regarding the module nameplate and terminal nameplate of XCU232H.

XCU232H



Module name plate



Terminal block name plate

Chapter 2 Specifications

2.1 Basic specifications

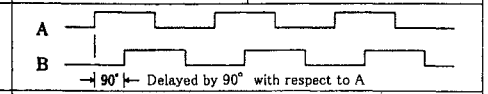
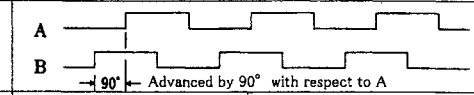
[Basic specifications (1/4)]

Item			Counter module XCU001H	2-CHANNEL Counter module XCU232H
Operating temperature			0 to 55 ℃	
Storage temperature			-10 to 75 ℃	
Operating relative humidity			20 to 90%RH (Non-condensing)	
Storage relative humidity			10 to 90%RH (Non-condensing)	
Current dissipation			0.3 A (5 V DC) 0.1 A (24 V DC)	0.16 A (5 V DC)
Dimensions			35W×210H×130D [mm]	
Mass			Approx. 500 g	
Input signal	Count pulse frequency		MAX. 50 kHz	MAX. 100 kHz/5 kHz (Possible change by switching) × 2 channels
	Input pulse voltage level		High: 6 – 12 V (Indicator: OFF) Low: 0 – 2 V (Indicator: ON)	Input voltage: 10 – 26 V 40 mA *1 × 2 channels Threshold value *2 : 1/2 of power voltage. (Possible change to 1/4)
	Count pulse width		ON: MIN. 5 μs OFF: MIN. 5 μs	ON: MIN. 4 μs OFF: MIN. 4 μs (At 80 μs, 5kHz)
	Marker pulse width		MIN. 10 μs	MIN. 10 μs (At 200 μs, 5kHz) The marker logic inversion function is available
	Input impedance		Approx, 20 kΩ (The built-in pull up resistor can be connected through the external wiring.)	
	Insulation		Photo-coupler	
	Number of pulse input points		3 points A: A phase, B: B phase, M: Marker } at one channel Phase difference (A-B) { +90° ±45° at forward { -90° ±45° at backward	
	External wiring		Shielded twisted pair cable	
	Polarity		Negative common (in the counter module)	

*1: 70 mA when built-in pull-up register is used.

*2: The threshold value is the boundary voltage value when the counter module detects the input pulse of high or low level.

[Basic specifications (2/4)]

Item			Counter module XCU001H	2-CHANNEL Counter module XCU232H
Input signal	2-phase input pulse	Increment (Count up)		
		Decrement (Count down)		
	Built-in battery (for input)		12 V DC ± 10 % (Output current: 50 mA MAX.) For the pulse encoder	-
Output signal	Output voltage		10 – 30 V DC	
	Load current		MAX. 0.5 A	
	Output mode		Transistor (Open collector)	
	Minimum load current		MIN. 1 mA	
	Output delay time	ON→OFF	MAX. 0.5 ms	
		OFF→ON	MAX. 0.5 ms	
	Voltage drop		MAX. 1.5 V (0.5 A)	
	Insulation		Photo-coupler	
	Number of output points		2 points (OUT1 and OUT2)	1 point / channel × 2 channels
	Leakage current		MAX. 0.1 mA	
	Polarity		Negative common (in the counter module)	
	External power supply for output *3		10 – 30 V DC Current consumption: 5 mA	10 – 30 V DC Current consumption: 5 mA × 2 channels
Function	Count range		0 – 65,535 (H0 · HFFFF)	0 – 4,294,967,295 (H0 · HFFFFFFFF)
	Count mode		· 2-phase pulse count mode (up, down) · Single-phase positive pulse, reverse pulse count mode (2-phase or single phase can be selected)	

*3: Current consumption is flows to the terminal block S0(S). Use different power supplies for input and output.

[Basic specifications (3/4)]

Item		Counter module	2-CHANNEL Counter module
		XCU001H	XCU232H
Function	Output	· 1 point / set value (Open collector) · Output retained if set value = counter value · Output if set value < counter value (Selectable)	· 1 point / channel × 2 channels · 1 point / 1 setting (Open collector) · Output is retained when comparison value equals the current value · Output when the comparison value less than the current value (Selectable)
	Marker	1 point (The counter value is reset directly by this signal.)	1 point (The counter value is reset directly by this signal.) × 2 channels
	LED Indication	· Counter value (in bits) · Outputs and pulse inputs.	{A, B, M, UP, DOWN, 1 ϕ /2 ϕ , >, =, Underflow, Overflow, CE, ME, OE, OUT} × 2 channels
	Registers	·Count register (UDC) ·1st set value register (CU(0)) ·2nd set value register (CU(1)) ·Write-data register ·Status register ·Control register	·32-bit read register (For reading the current and comparison values) ·32-bit write register (For reading the current and comparison values) · Status registers 1 and 2 · Control registers 1 and 2

[Basic specifications (4/4)]

Item		Counter module	2-CHANNEL Counter module
		XCU001H	XCU232H
Function	Function	·Presetting of count value · Reading of count value ·Writing of set value ·Reading of status Set value = Counter value (Latch or level signal) Set value < Counter value (Level signal) Overflow flag (Latch or level signal) Underflow flag (Latch or level signal)	·Current value setting ·Current value read · Comparison value setting · Comparison value read ·Status read Comparison value = Current value (Latch) Comparison value < Current value (Level) Overflow flag (Latch) Underflow flag (Latch) CPU STOP Countable/ Uncountable setting (no output during CPU STOP)

[Note] Input pulse threshold value voltage table for XCU232H
(Power voltage is E)

XCU232H

Terminal block level \ 4 or 8 of SW1	ON	OFF
High → Low	0.19 to 0.24E	0.41 to 0.47E
Low → High	0.28 to 0.33E	0.49 to 0.57E

[Reference] Comparison between XCU001H and XCU232H Counter Modules

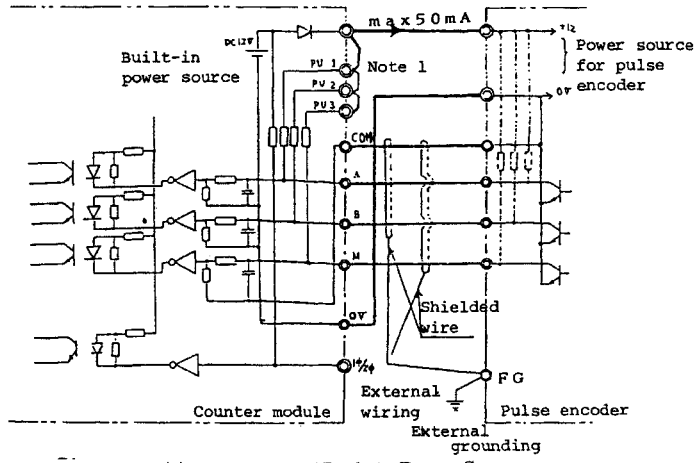
	XCU001H	XCU232H
Number of quantities	1	2
Number of count bits	16	32/quantity
Count frequency	50 kHz (maximum)	100 kHz (maximum) (can be set to 5 kHz (maximum))
Marker logic	Negative logic	Negative or positive logic
Power supply for input	Built-in (12 V)	External feed (10 to 26 V)
Number of identity output points	2	1/channel
LED display	Input, output, and current value	Input, output, up, down, and status register contents, etc.
CE (count enable)	Unavailable	Available
OE (output enable)	Unavailable	Available

2.2 Input/Output Interface

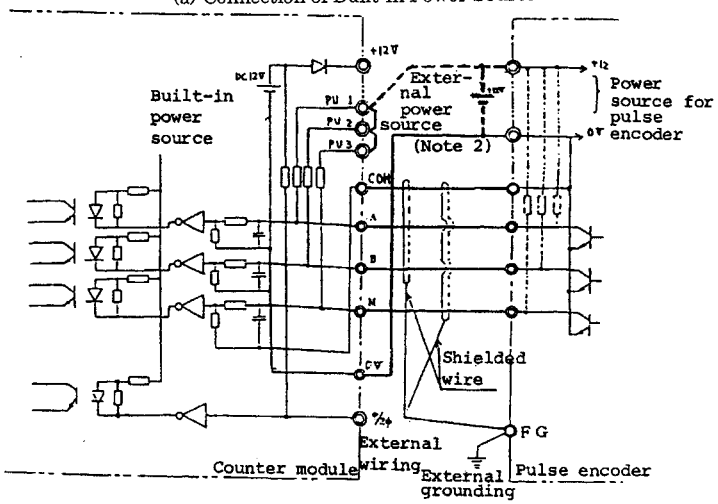
(1) XCU001H

XCU001H

【Input Interface】



(a) Connection of Built-in Power Source

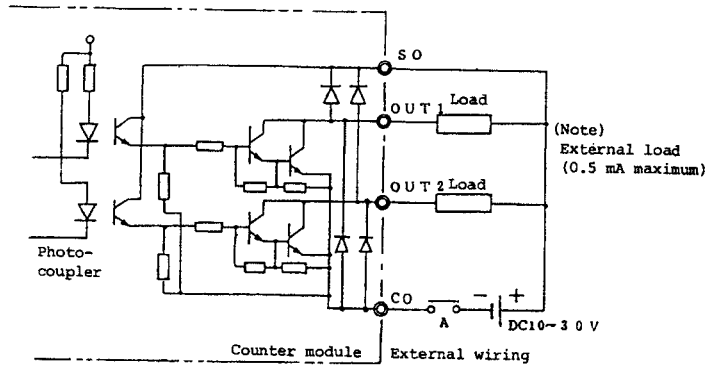


(b) Connection of External Power Source

Note 1: In case of an open-collector output of the pulse encoder, connect the PU1 to PU3 terminals to the +12 V terminal as shown in above.
Note 2: If the pulse encoder requires a current greater than 50 mA, connect the external power source as shown by dotted lines. (12 V DC ±10%) Leave the +12 V terminal of the counter module disconnected from the +12 V terminal of the pulse encoder.

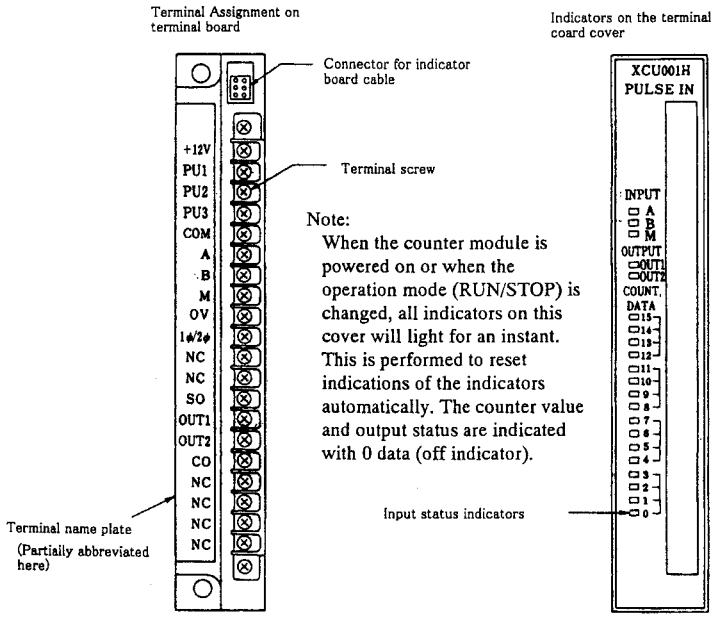
【Output Signal (OUT1 and OUT2)】 XCU001H

When using the output signals (OUT1 and OUT2), notice that they are output according to pulse input even when CPU is off.
If it is undesirable that the output signals are output when CPU is off, insert a contact output (A in the figure below) into the common side of the output as shown in the figure below.



OUT1: Outputs the result of comparison between the counter value and the first set-value register CU(0).
OUT2: Outputs the result of comparison between the counter value and the second set-value register CU(1).

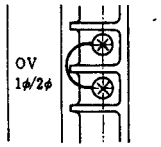
【Terminal Board and Indicators】 XCU001H



Note:
When the counter module is powered on or when the operation mode (RUN/STOP) is changed, all indicators on this cover will light for an instant. This is performed to reset indications of the indicators automatically. The counter value and output status are indicated with 0 data (off indicator).

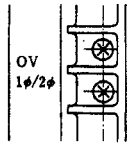
【Count pulse selection (1-phase or 2-phase)】

Selection of 1-phase pulse



Short-connect these terminals

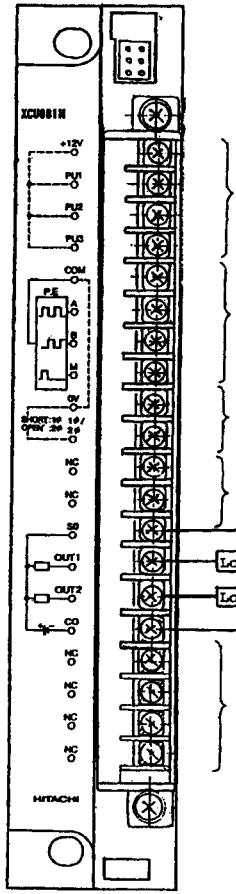
Selection of 2-phase pulse



Leave these terminals

0V and 1φ/2φ terminal is change the 1-phase pulse / 2-phase pulse. Leave these terminals open when a 2-phase pulse is used. Connect these pins when a 1-phase pulse is used.

XCU001H



Connect these terminals to the +12 V terminal of the pulse encoder if the encoder is of an open-collector output type.

Leave these terminals unconnected if the encoder is of a voltage output type.

Connect these terminals to the following terminals of the pulse encoder:
A : Phase-A output
B : Phase-B output
M : Marker signal

Leave these terminals open when a 2-phase pulse is used.

Connect these pins when a 1-phase pulse is used.

Reserved (Note)

Load
Load
External load (0.5 A maximum)
+ DC 10 – 30 V
– External power source

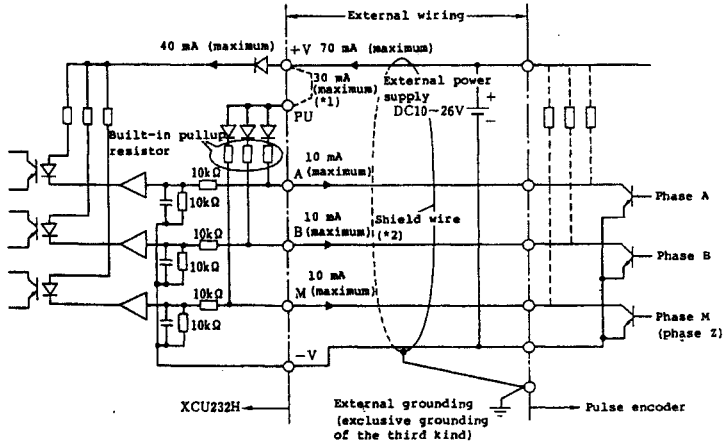
Reserved (Note)

(Note)
Do not connect any wiring to these reserved terminals.

(2) XCU232H

XCU232H

【Input Interface (One Channel)】

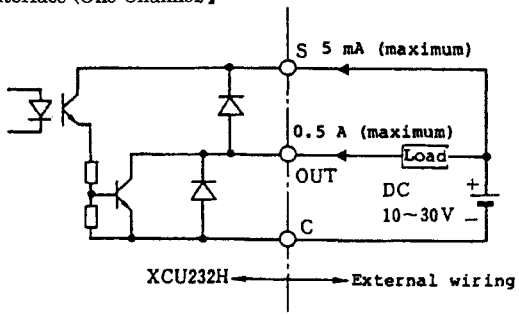


*1 When using the built-in pullup resistor, strap this part. To use this resistor, the pulse encoder side must pull in current of 10 mA.

The pullup resistor is not used when the pulse encoder side is for voltage output.

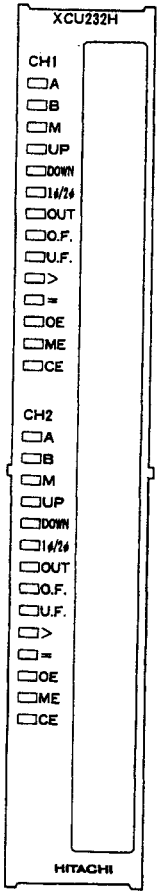
*2 Use a paired common shield wire. Each +V, A, B, or M wiring should be paired with -V.

【Output Interface (One Channel)】



【Functions of LED Display Section】

XCU232H



(1) A, B, and M lamps

Indicate the terminal block levels of phases A, B, and M.
When the terminal block level goes high, the corresponding phase lamp comes out. When it goes low, the corresponding phase lamp comes on.

(2) UP and DOWN lamps

The UP or DOWN lamp comes on according to the current count status.
Both the UP and DOWN lamps are off till a pulse is input after the power supply has been turned on. When the counter stops counting, the immediately preceding count status is displayed.

(3) 1ø/2ø lamp

Indicates the type of input pulse setting.
When two-phase input is set, the 1ø/2ø lamp comes out.
When sigle-phase input is set, this lamp comes on. Use switch SW2 to set this.

(4) OUT lamp

The OUT lamp comes on when the identity output is on.

(5) O.F. and U.F. lamps (*1)

When the overflow flag is set to 1, the O.F. lamp comes on. When the underflow flag is set to 1, the U.F. lamp comes on.

(6) > lamp (*1)

The > lamp comes on when the current value exceeds the comparison value.

(7) = lamp (*1)

The = lamp comes on when the current value equals the comparison value.

(8) OE, ME, and CE lamps (*1)

When the identity output is enabled, the OE (output enable) lamp comes on. When the marker input is enabled, the ME (marker enable) lamp comes on. When counting is enabled, the CE (count enable) comes on.

*1 The explanations of 5 to 8 correspond to those of status register (1).

2.3 Setting of XCU232H

Be sure to set the following items before using the XCU232 module. Use SW1 and SW2 to set these items.

【Items to be set】

XCU232H

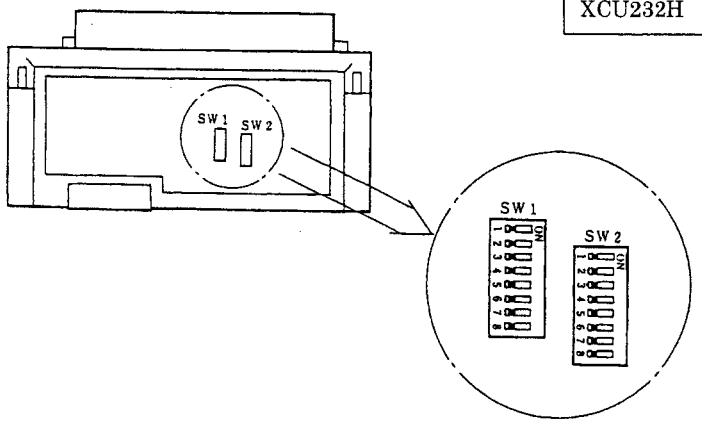
	Item to be set		Switch	Switch No.	ON	OFF
1	Maximum count frequency	First channel	SW1	1 - 3	5 kHz	100 kHz
		Second channel	SW1	5 - 7		
2	Input voltage threshold value	First channel	SW1	4	1/4 of external power voltage	1/2 of external power voltage
		Second channel	SW1	8		
3	CPU stop count	First channel	SW2	1	Needed	Not needed
		Second channel	SW2	5		
4	Input pulse format	First channel	SW2	2	Single phase	Two phase
		Second channel	SW2	6		
5	Marker logic	First channel	SW2	3	Positive logic	Negative logic
		Second channel	SW2	7		
6	Ring counter (*1)	First channel	SW2	4	Used	Not used
		Second channel	SW2	8		

*1 Before using the ring counter, be sure to set switch No. 3 (first channel) and switch No. 7 (second channel) of SW1 to OFF.

[Switch locations]

SW1 and SW2 are mounted on the locations shown in the figure below.

XCU232H



[Details of Items to be set]

(1) Maximum count frequency

SW1 can be used to change the maximum count frequency. When SW1 is set to OFF, the maximum count frequency is set to 100 kHz. When SW1 is set to ON, it is set to 5 kHz. When the input pulse frequency is 5 kHz or below, set SW1 to ON because the influence by external noise, etc., is lessened.

(2) Input voltage threshold value

When the voltage (10 to 26 V) of the input power supply equals the input pulse voltage, set to SW1 to OFF because the influence by external noise, etc., is lessened.

When the input pulse voltage is 5 V, set the voltage of the input power supply to 10 V and SW1 to ON. This sets the threshold value to 2 to 3 V and enables counting (see Table 3.2). The pulse output side, however, needs a pressure of at least 10 V.

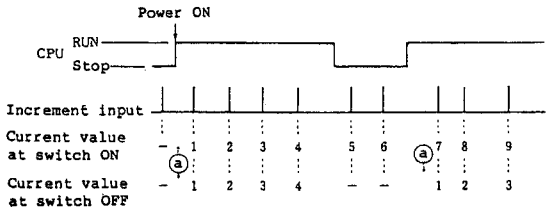
XCU232H

(3) CPU stop count (*1)

To start counting from the value preset when the CPU was started (that is, the counter is not incremented or decremented during CPU stop), set SW2 to OFF.

To continue counting irrespective of CPU stop or running, set SW2 to ON. The identity output, however, is not set to ON during CPU stop because OE (output enable) is 0.

Operation comparison at switch ON/OFF



– indicates that data is undefined.

ⓐ indicates that the user program clears the current value (0) and performs CE (count enable). Counting is possible when CE is 1.

*1 When SW2 is set to ON, CE (count enable) and ME (marker enable) is 1 (count enabled, marker valid) irrespective of CPU stop or running. The LED does not come on.

When the user program performs CE or ME, the LED comes on or off but the operation continues the ON status. Note that the LED display differs from the actual operation.

(4) Input pulse format

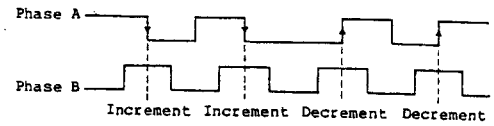
To input a two-phase pulse, set SW2 to OFF. If phase A falls when phase B is High, the counter is incremented. When phase A rises, the counter is decremented.

To input a single-phase pulse, set SW2 to ON. Phase A is used for increment input and phase B for decrement input.

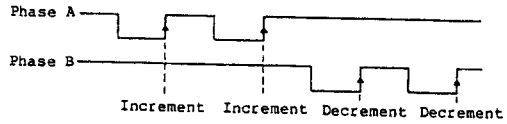
The counter is incremented or decremented at the rising edge of the each pulse.

XCU232H

At two-phase pulse (switch OFF)



At single-pulse (switch ON)



(5) Marker logic

To make the marker signal valid (negative logic) when the marker (M) input goes Low, set to SW2 to OFF.

To make the marker signal valid (positive logic) when the marker (M) input goes High, set to SW2 to ON.

(6) Ring counter (see Section 9.2 "Example of Ring Counter")

The ring counter starts increment from value A, and when the current value reaches value B (B > A), it repeats return of the current value to value A.

To enable this return operation, set SW2 to ON and specify the identify output (> setting) in the marker (M) input.

Value A changes to the value DY□□n6 and value B to the value set in the comparison value.

When the 1-channel and 2-channel counters are used as the ring counter, value A is common to the first and second channel because common resistor DY□□n6 is used. Value B can be determined per channel.

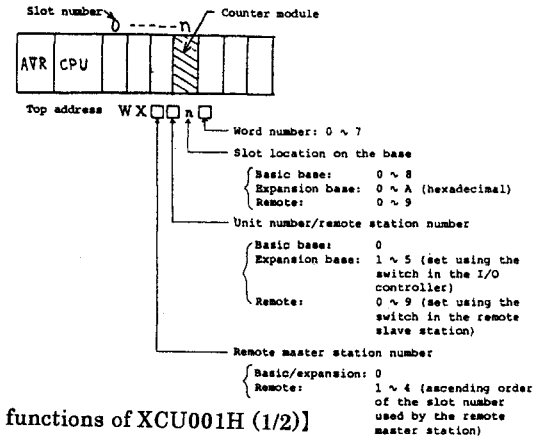
The ring counter uses the identity output. Note that if the input pulse becomes fast due to delay of the identity output, an error may occur.

To use this function in the first channel, be sure to set switch No. 3 of SW1 to OFF. To use the function in the second channel, be sure to set switch No. 7 of SW1 to OFF.

2.4 I/O assignment and Registers

The H-series counter module 'XCU001H, XCU232H) uses an 8-word (128bits) area The four words (64 bits) of the area are used for inputs (as a read-only area) and the remaining four words (64 bits) are used for output (as a write-only area). The content of each register (except the status register) must be coded in words.

(1) Assignment of I/O number to the counter module



[Resister functions of XCU001H (1/2)]

(2) I/O numbers and register of functions

XCU001H

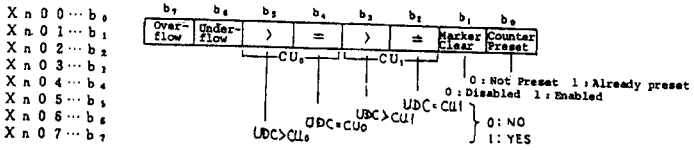
I/O number	(bit) b15 … b8 b7 … b0
WX□□n 0	Status register
WX□□n 1	Current count value (UDC) (16 bits)
WX□□n 2	(Reserved)
WX□□n 3	(Reserved)
WY□□n 4	Control register (8 bits)
WY□□n 5	Data to be written in the counter (16 bits)
WY□□n 6	1st set-value register (CU0) (16 bits)
WY□□n 7	2nd set-value register (CU1) (16 bits)

Note: The contents of all registers in the counter module are reset to zeros when the counter module is powered on and when the operation mode (RUN/STOP) is changed.

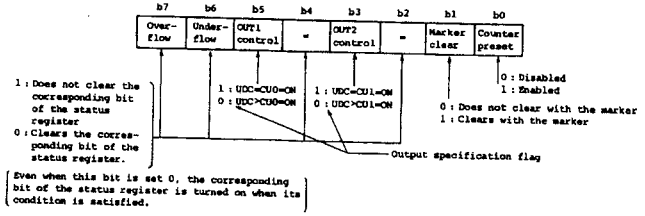
The status register indicates the status of each register (comparison between preset value and counter value, marker input, count underflow, and count overflow), using flags. Higher bits b8 to b15 are always 1s.

Bit I/O number

Note: b5, b3, b2, b0: Level signal
b7, b6, b4, b2: Level signal if its value is 0 and latch signal if its value is 1



(4) Control register (Write area)
The control register specifies the operation of the counter module (by the user). The control register is formatted as follows:



I/O allocation

WX□□n0	Status register (1)
1	Status register (2)
2	Low-order read data
3	High-order read data
WY□□n4	Control register (1)
5	Control register (2)
6	Low-order set data
7	High-order set data

(1) WX□□n0 (status register (1))

	Not used	Second channel							Not used	First channel						
		Over-flow	Under-flow	>	=	OE	ME	CE		Over-flow	Under-flow	>	=	OE	ME	CE
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

CE (bits 0 and 8): Indicates whether the count is enabled or disabled. When bit 0 or 8 is 1, the counter can count. When bit 0 or 8 is 0, the counter cannot count. When it is 0, the counter also does not count even if a pulse is input.

ME (bits 1 and 9): Indicates whether the marker is enabled or disabled. When bit 1 or 9 is 1, the marker is enabled. When bit 1 or 9 is 0, the marker is disabled. When it is 0, the marker does not operate even if a pulse is input.

OE (bits 2 and 10): Indicates whether the output is enabled or disabled. When bit 2 or 10 is 1, the output is enabled. When bit 2 or 10 is 0, the output is disabled. When it is 0, no data is output even if the identify output condition is satisfied.

= (Bits 3 and 11): Bit 3 or 11 is set to 1 when the count current value equals the comparison value. 1 is retained even if the count current value changes. To reset the flag set to 1, to 0, set clear bit 67 or 75 of control register (1) to 1.

> (bits 4 and 12): Bit 4 or 12 is set to 1 when the count current value exceeds the comparison value. 1 is retained when this condition is satisfied. When this condition is dissatisfied, bit 4 or 12 is set to 0.

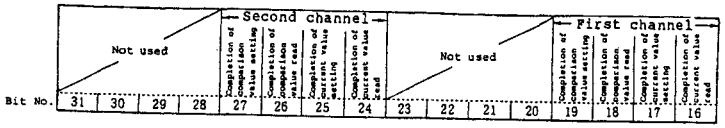
Underflow:
(bits 5 and 13)

Bit 5 or 13 is set to 1 when the count current value becomes "HFFFFFFFF". The counter is decremented when the counter current value becomes 0, with the underflow clear flag (bit 69 or 77) set to 1. To reset the flag set to 1, to 0, set bit 69 or 77 (underflow clear flag) of control register (1) to 0.

Overflow:
(bits 6 and 14)

Bit 6 or 14 is set to 1 when the count current value becomes 0. The counter is incremented when the counter current value becomes "HFFFFFFFF", with the overflow clear flag (bit 70 or 78) set to 1. To reset the flag set to 1, to 0, set bit 70 or 78 (overflow clear flag) of control register (1) to 0.

(2) WX□□n1 (status register (2))



Completion of current value read (bits 16 and 24):

Bit 16 or 24 is set to 1 when read of the current value (comparison value) is specified in control register (2) and the current value (comparison value) is set in DX n2. When bit 16 or 24 is set to 1, the value set in DX□□n2 is read.

Completion of comparison value read (bits 18 and 26):

Bit 18 or 26 is set to 0 when the corresponding flag of control register (2) is set to 0. The value in DX□□n2 becomes undefined.

Completion of current value setting (bits 17 and 25):

Bit 17 or 25 is set to 1 when setting the current value (comparison value) is specified in control register (2) and setting the current value (comparison value) in DY□□n6 is completed.

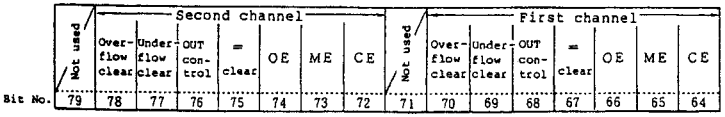
Completion of comparison value setting (bits 19 and 27):

Bit 19 or 27 is set to 0 when the corresponding flag of control register (2) is set to 0.

(3) WX□□n2 (low-order read data)
WX□□n3 (high-order read data) } DX□□n2

The current and comparison values to be read are set in these registers. Double word DX□□n2 can be used to read 32-bit data once. Data is set only when the corresponding read flags of control register (2) are 1.

(4) WY□□n4 (control register (1))



CE (bits 64 and 72): The counter counts the input pulse only when bit 64 or 72 is 1.

ME (bits 65 and 73): Marker input is acceptable only when bit 65 or 73 is 1.

OE (bits 66 and 74): The identity output is enabled only when bit 66 or 74 is 1.

= clear:
(bits 67 and 75) Bit 67 or 75 is set to 1 when the = flag (bit 3 or 11) of status register (1) is set to 0. The = flag of status register (1) retains 0 when bit 67 or 75 is 1 because these bits operate according to the level.

OUT control:
(bits 68 and 76) Bit 68 or 76 is used to select the identity output condition. When bit 68 or 76 is 0, the identity output is enabled when the current value exceeds the comparison value. When bit 68 or 76 is 1, the identity output is enabled when the current value equals the comparison value.

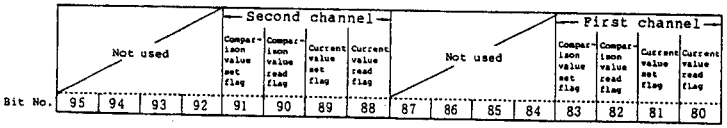
Underflow clear: (bits 69 and 77)

Bit 69 or 77 is set to 0 when the underflow flag (bit 5 or 13) of status register (1) is set to 0. The underflow flag of status register (1) retains 0 when bit 69 or 77 is 0 because these bits operate according to the level. To use the underflow flag, set bit 69 or 77 to 1.

Overflow clear: (bits 70 and 78)

Bit 70 or 78 is set to 0 when the overflow flag (bit 6 or 14) of status register (1) is set to 0. The overflow flag of status register (1) retains 0 when bit 70 or 78 is 0 because these bits operate according to the level. To use the overflow flag, set bit 70 or 78 to 1.

(5) WY□□n5 (control register (2))



Current value read flag (bits 80 and 88) and comparison value read flag (bit 82 to 90):

To read the current value, set the current value read flag to 1. To read the comparison value, set the comparison value read flag to 1. The current value is read at the rising edge (0 → 1) of the current value read flag. The comparison value is read also at the rising edge (0 → 1) of the comparison value read flag. Read data can be retained in DX□□n2 only when the current or comparison value read flag is 1. Two or more read flags cannot be set to 1 at a time.

Read data is undefined if two or more read flags are set to 1. If two or more read flags are set to 1, read data in the following sequence:

First read data for the first read flag and set the flag to 0. After confirming that the corresponding read completion flag of status register (2) has been set to 0, set the second read flag to 1 and read data.

Current value set flag (bits 81 and 89) and comparison value set flag (bits 83 and 91):

To set the current value, set the current value set flag to 1. To set the comparison value, set the comparison value set flag to 1. The current value is set at the rising edge (0 → 1) of the current value set flag. The comparison value is set also at the rising edge (0 → 1) of the comparison value set flag. The data to be set is the value in DY□□n6. If two or more set flags are set to 1, the same data is set in all the fields corresponding to 1.

(6) WY□□n6 (low-order set data)
WY□□n7 (high-order set data)
} DY□□n6

The current and comparison values to be set are written in these registers. Double word DY□□n6 can be used to write 32-bit data once.

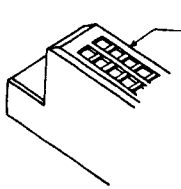
Chapter3 Mounting and Precautions

3.1 Mounting

- Counter module (XCU001H, XCU232H) can be installed in both the basic and expansion bases (including the remote destination).
- Take care to act on the following points when the Counter module is mounted.

(1) Confirm the following two points when mounting or dismounting the Counter module.

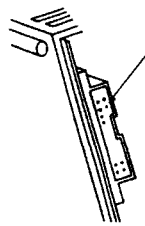
(i) Check the connections of the Counter module's connector in basic base side.



Check that the dividing plate on module is normal.

⇨ If there are any problems, contact nearest after-sales service station or your dealer.

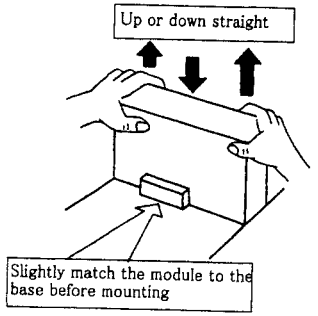
(ii) Check the connections of the Counter module contacting with the base.



Check the bend of the pin.

⇨ If there are any problems, contact nearest after-sales service station or your dealer.

(2) Mount or dismount the Counter module straight as shown in the figure below.



Up or down straight

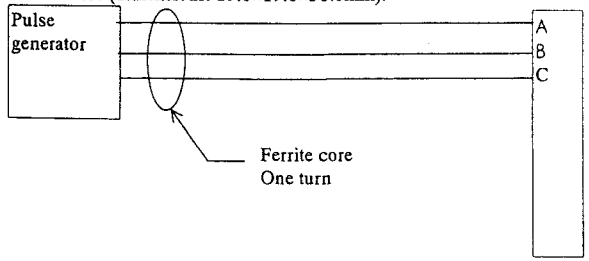
Slightly match the module to the base before mounting

⇨ Do not set the Counter module forcibly when the connectors cannot be inserted easily. Check that there is no defect such as described in (ii) above.

To mount the module, slightly and straight match each connector together and push the top of the case by means of hand so that the connectors are set closely.

3.2 Precautions

- Counter module is a high-speed module that responds to the maximum count frequency of 100kHz (XCU232H) or 50kHz (XCU001H). For input wiring installation, fully consider separation with other wirings because if a noise, etc., infiltrate into the input signal, an error count may occur.
- If the input frequency is high, the input pulse weakens due to the length and type of wiring and drive capacity of the pulse output side, etc. If the input pulse weakens, the input signal may not be sent to the counter module correctly.
- Turn off the power supply before mounting and dismounting the module or terminal block and connecting the external wiring.
- Carry out the following instructions to meet with EMC regulation for counter modules. (XCU001H and XCU232H)
  - Use shielded cable and connect shield to FG.
  - Use ferrite cores to communication lines to the twist pair cables.
  - The twist pair cables must be in the metal duct.
  - Route the I/O lines as close as possible to grounded surfaces such as cabinet elements, metal bars and cabinets panels.
  - Separate from the other power and signal lines.
  - Use a ferrite core (dimensions: 19.0×19.0×30.0mm).



Counter module (XCU001H/XCU232H)

- Use a shield wire to lay out the external wiring of the counter module in a place different from where other power and signal lines of different from where other power and signal lines of different voltage s are connected. Also ground one side of the shield wire in the pulse encoder side.
- Depending on noise environment, however, apply both-end grounding or non-grounding.
- When routing the twisted pair cables for Counter, along a path different from other power lines and signal lines or use a metal pipe to reduce external noise and assure high reliability.

Besides, in detail as occasion demands please see the instruction manual of Counter module (XCU001H: NB973*(X): separate account, XCU232H: NB3111*(X): separate account).